

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

THOMAS FEUDEL  
MANFRED HORSTMANN  
ROLF STEPHAN

Group Art Unit: Unknown

Examiner: Unknown

Serial No.: Unknown

Att'y Docket: 2000.106300/DE0106

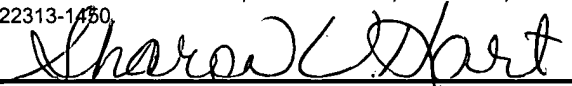
Filed: Concurrently Herewith

For: SEMICONDUCTOR DEVICE HAVING  
IMPROVED DOPING PROFILES AND  
A METHOD OF IMPROVING THE  
DOPING PROFILES OF A  
SEMICONDUCTOR DEVICE

**SUBMISSION OF PRIORITY DOCUMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

EXPRESS MAIL RECEIPT	
NUMBER:	EV 291395748 US
DATE OF DEPOSIT:	June 23, 2003
I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
	
Signature	

Transmitted for filing herewith is the certified copy of the priority document – German Patent Application No. 102 61 374.5 filed on December 30, 2002.

If any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason relating to the enclosed materials, the Assistant Commissioner is authorized to said fees Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0106.

Please date stamp and return the accompanying postcard to evidence receipt of this document.

Date: June 23, 2003



23720  
PATENT TRADEMARK OFFICE

Respectfully submitted,

A handwritten signature in black ink, appearing to read "J. Mike Amerson", written over a horizontal line.

J. Mike Amerson  
Reg. No. 35,426  
WILLIAMS, MORGAN & AMERSON  
10333 Richmond, Suite 1100  
Houston, Texas 77042  
(713) 934-4055  
(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS

# BUNDESREPUBLIK DEUTSCHLAND



## Prioritätsbescheinigung über die Einreichung einer Patentanmeldung

**Aktenzeichen:** 102 61 374.5

**Anmeldetag:** 30. Dezember 2002

**Anmelder/Inhaber:** ADVANCED MICRO DEVICES, INC.,  
Sunnyvale, Calif./US

**Bezeichnung:** Semiconductor device having improved doping  
profiles and a method improving the doping  
profiles of a semiconductor device

**IPC:** H 01 L 21/336

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der  
ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 28. April 2003  
**Deutsches Patent- und Markenamt**  
Der Präsident  
Im Auftrag

A handwritten signature in black ink, appearing to read 'Hiebinger', written over a horizontal line.

Hiebinger

GRÜNECKER KINKELDEY, STOCKMAIR & SCHWANHÄUSSER

ANWALTSSOZIELTÄT



GKS & S MAXIMILIANSTRASSE 58 D-80538 MÜNCHEN GERMANY

RECHTSANWÄLTE  
LAWYERS

MÜNCHEN  
DR. HELMUT EICHMANN  
GERHARD BARTH  
DR. ULRICH BLUMENRÖDER, LL. M.  
CHRISTA NIKLAS-FALTER  
DR. MAXIMILIAN KINKELDEY, LL. M.  
DR. KARSTEN BRANDT  
ANJA FRANK, LL. M.  
UTE STEPHANI  
DR. BERND ALLEKOTTE, LL. M.  
DR. ELVIRA PFRANG, LL. M.  
KARIN LOCHNER  
BABETT ERTLE

PATENTANWÄLTE  
EUROPEAN PATENT ATTORNEYS

MÜNCHEN  
DR. HERMANN KINKELDEY  
PETER H. JAKOB  
WOLFHARD MEISTER  
HANS HILGERS  
DR. HENNING MEYER-PLATH  
ANNELE EHNOLD  
THOMAS SCHUSTER  
DR. KLARA GOLDBACH  
MARTIN AUFENANGER  
GOTTFRIED KUTZSCH  
DR. HEIKE VOGELSANG-WENKE  
REINHARD KNAUER  
DIETMAR KUHLE  
DR. FRANZ-JOSEF ZIMMER  
BETTINA K. REICHELT  
DR. ANTON K. PFAU  
DR. UDO WEIGELT  
RAINER BERTRAM  
JENS KOCH, M. S. (J of PA) M. S.  
BERND ROTHAEDEL  
DR. DANIELA KINKELDEY  
THOMAS W. LAUBENTHAL  
DR. ANDREAS KAYSER  
DR. JENS HAMMER  
DR. THOMAS EICKELKAMP

PATENTANWÄLTE  
EUROPEAN PATENT ATTORNEYS

BERLIN  
PROF. DR. MANFRED BÖNING  
DR. PATRICK ERK, M. S. (MIT)  
  
KÖLN  
DR. MARTIN DROPMANN  
  
CHEMNITZ  
MANFRED SCHNEIDER

OF COUNSEL  
PATENTANWÄLTE

AUGUST GRÜNECKER  
DR. GUNTER BEZOLD  
DR. WALTER LANGHOFF  
  
DR. WILFRIED STOCKMAIR  
(-1996)

IHR ZEICHEN / YOUR REF.

UNSER ZEICHEN / OUR REF.

DATUM / DATE

P 32919-04553/we

30.12.02

**Applicant: ADVANCED MICRO DEVICES, INC.**

**One AMD Place, Mail Stop 68,  
Sunnyvale, CA 94088-3453  
USA**

**SEMICONDUCTOR DEVICE HAVING IMPROVED DOPING PROFILES  
AND A METHOD OF IMPROVING THE DOPING PROFILES OF A  
SEMICONDUCTOR DEVICE**

GRÜNECKER KINKELDEY  
STOCKMAIR & SCHWANHÄUSSER  
MAXIMILIANSTR. 58  
D-80538 MÜNCHEN  
GERMANY

TEL. +49 89 21 23 50  
FAX (GR 3) +49 89 22 02 87  
FAX (GR 4) +49 89 21 86 92 93  
<http://www.grunecker.de>  
e-mail: [postmaster@grunecker.de](mailto:postmaster@grunecker.de)

DEUTSCHE BANK MÜNCHEN  
No. 17 51734  
BLZ 700 700 10  
SWIFT: DEUT DE MM

31.03.03

# **SEMICONDUCTOR DEVICE HAVING IMPROVED DOPING PROFILES AND A METHOD OF IMPROVING THE DOPING PROFILES OF A SEMICONDUCTOR DEVICE**

## **FIELD OF THE PRESENT INVENTION**

The present invention relates to the fabrication of integrated circuits, and more particularly relates to the implanting of ions of dopant materials into workpieces and/or substrates suitable for the fabrication of integrated circuits. More specifically, the present invention relates to a method of amorphizing a crystalline substrate on which integrated circuits are fabricated.

## **DESCRIPTION OF THE PRIOR ART**

In the last several years, the numbers of circuit elements manufactured on semiconductor substrates has continuously grown and the size of the circuit elements has continuously decreased, accordingly. Presently, circuit elements are commonly fabricated featuring minimum sizes less than  $0.18\mu\text{m}$  and the progress in the manufacturing technology seems likely to continue to proceed in this manner.

However, in the case of field-effect transistors, as process technology improved to the point where devices could be fabricated with a gate length less than  $2\mu\text{m}$ , the need arose to restrict the doping profiles of the several implants carried out during the manufacturing process to shallow locations. That is, implantations need to be confined within shallow well predefined regions. To obtain the shallow doping profiles required for, for instance, halo structures, source/drain regions and channels, all physical mechanisms allowing dopants to penetrate into the substrate must be strictly controlled or eliminated.

In particular, the principle factor to be controlled is ion-channeling.

To accomplish this end great efforts have been made and several measures have been taken in the art. Among these measures, common manufacturing processes often use a so-called "pre-amorphization" implantation step before carrying out the usual dopant implantation steps. In particular, an amorphous zone is usually formed

during a first pre-amorphization implantation and, during subsequent implantation processes the doped regions (halo and source/drain extension regions) are formed. Normally, heavy inert ions like Germanium or Xenon are implanted at an implant energy of approximately 80-200 keV to fully amorphize the surface regions of the substrate.

In the following, a description will be given with reference to Figures 1a to 1d of a typical prior art process for forming the active regions of a field-effect transistor, including a typical "pre-amorphization" implanting step as well as a typical "halo" implanting step and the implanting steps for forming the source and drain regions.

Figure 1a schematically shows a MOS transistor 100 to be formed on a substrate 1, such as a silicon wafer. Isolation structures 2 define an active region of the transistor 100. Moreover, reference 3 relates to a polysilicon gate electrode of the MOS transistor 100. Reference 6 denotes a gate insulation layer. Reference 7a relates to an ion beam to which the substrate 1 is exposed during a "pre-amorphization" implanting process, and reference 5a relates to amorphous regions formed into the substrate 1.

In Figures 1b to 1d, those parts already described with reference to Figure 1a are identified by the same reference numerals. In addition, in Figure 1b, reference 7h relates to an ion beam to which the substrate 1 is exposed for forming the halo regions 5h. The dopant material implanted during such a process is of the same type as the dopant used for doping the substrate. That is, the halo implants for NMOS and PMOS devices are performed using a P-type and a N-type dopant material, respectively. In a sense, the halo implants reinforce the dopants in the substrate.

In Figure 1c, reference 7e relates to an ion beam to which the substrate 1 is exposed for forming the source/drain extension regions of the transistor 100. Moreover, references 5'S and 5'D relate to the source extension region and the drain extension region, respectively of the transistor 100. Still in Figure 1c, reference e relates to a portion of the transistor 100 which is depicted in enlarged view in Figure 1c', in which corresponding reference numerals identify corresponding parts already described with reference to Figure 1c.

In Figure 1d, reference 4 relates to dielectric sidewall spacers formed on the sidewalls of the polysilicon line 3 and references 5S and 5D relate to the source and drain regions, respectively, after a further heavy implantation step has been carried out for determining the final concentration of dopants in the source and drain regions. Finally, in Figure 1d reference 7SD identifies an ion beam to which the substrate 1 is exposed for forming the source and drain regions 5S and 5D.

A typical process flow for forming the active regions of the transistor 100 comprising the amorphous regions 5a, the halo structures 5h and the source and drain regions 5S and 5D may include the following steps.

Following the formation of the gate insulation layer 6 and the overlying polysilicon line 3 according to well known lithography and etching techniques, the amorphous regions 5a are formed during a first pre-amorphization implantation step (see Figure 1a). To this end, the substrate 1 is exposed to the ion beam 7a and heavy ions such as, for example, Phosphorous (P) Arsenic (As), and Argon (Ar) are implanted into the substrate at an implanting energy of about 80 keV. The ion beam 7a is normally kept perpendicular or at a weak tilt angle (up to  $10^\circ$ ) with respect to a direction perpendicular to the surface of the substrate 1.

It has been observed that at a predefined implanting dose, local amorphous regions are created by the ions penetrating into the substrate, which eventually overlap till a continuous amorphous layer is formed.

This amorphous layer (or the amorphous regions 5a) is formed with the purpose of controlling ion channeling during the next implanting steps so as to obtain shallow implanting profiles for both the halo regions and the source and drain regions to be formed in a substrate. That is, the implanted ions do not penetrate in an amorphous layer as deeply as in a crystalline layer so that the implanted ions can be confined to shallower regions and the actual doping profile and final dopant concentration of those regions implanted after the pre-amorphization implantation step can be better controlled. However, due to the fact that the amorphous regions 5a are formed with a non or weakly tilted implantation beam, only the vertical penetration depth of subsequent doping profiles can be reduced.

In a next step as depicted in Figure 1b, the halo regions 5h of the transistor 100 are formed. In particular, a further ion implantation step is carried out during which the substrate is exposed to an ion beam 7h. As depicted in Figure 1b, during the depicted halo implant the ion beam 7h is kept perpendicular with respect to a direction perpendicular to the surface of the substrate 1 or the ion beam 7h is weakly tilted (up to  $10^\circ$ ) with respect to the surface of the substrate 1. The dopant concentration in the regions 5h as well as the implant energy of the dopants are selected depending on the type of transistor to be formed on the substrate 1. For instance, boron ions in NMOS and phosphorous ions in PMOS are implanted to form a halo punch-through suppression region in each device. Usually, boron implanted at 90 keV with a dose of  $2 \times 10^{13} \text{ cm}^{-2}$ . Similar procedures are used for implanting phosphorous.

A thermal treatment such as an annealing step is usually performed after the ion implantation step for diffusing dopants into the substrate.

As apparent from Figure 1d, the halo regions 5h, in correspondence of the edges of the polysilicon line 3 and the gate 6 extend outside the amorphous zones 5a. This is due to the fact that during the implantation steps for forming the amorphous zones 5a, the ion beam is kept substantially perpendicular with respect to the surface of the substrate 1, so that the edges of these amorphous regions 5a are substantially aligned with the edges of the gate 6. Accordingly, ion-channeling during the subsequent implantation steps for forming the halo structures 5h cannot be adequately controlled in the horizontal direction or, in other words, the doping profile of the halo regions 5h cannot be kept as shallow as desired in the horizontal direction but portions of the halo regions are formed extending beyond the amorphous regions 5a.

During a next step as depicted in Figure 1c, a third ion implantation step is carried out to form the source/drain extension regions 5'S and 5'D. To this end, by exposing the substrate 1 to an ion beam 7e, a dose of approximately  $3 \times 10^{13} - 3 \times 10^{14} \text{ cm}^{-2}$  dopant ions is implanted at low energy (3 to 5 keV). This third ion implantation step is performed with N-type and P-type dopant materials for NMOS and PMOS devices, respectively. The problem arising during the halo implantation step of Figure 1b, namely that ion channeling cannot be adequately controlled in the horizontal direction, arises during the ion implantation step of 1c as well. Accordingly, the



source and drain regions 5'S and 5'D cannot be contained inside the amorphous regions 5a previously formed but portions of the source and drain regions 5'S and 5'D extend beneath the layer 6 and the overlying polysilicon line 3, especially after a heat treatment process is performed. Accordingly, also the doping profiles of the source and drain regions 5'S and 5'D cannot be kept as shallow as desired in the horizontal direction.

In particular, the situation after the implanting step of Figure 1c is that depicted in enlarged view in Figure 1c', with the doping profiles of both the source and drain extension regions 5'S and the halo regions 5h extending beyond the doping profile of the amorphous 5a, in correspondence of the edges of the layer 6 and the overlying polysilicon line 3.

During a subsequent step, the source and drain regions 5S and 5D of the transistor 100 are completed as depicted in Figure 1d. In particular, dielectric sidewall spacers 4 are formed on the sidewalls of the polysilicon line 3 according to well-known techniques and a further heavy implantation step is carried out for implanting dopants into those regions of the substrate not covered by the polysilicon line 3 and the sidewall spacers 4. At the end of the heavy implantation step, the source and drain regions 5S and 5D are formed to exhibit the desired dopant concentration. For NMOS and PMOS type devices, this heavy implantation step is performed using a N-type and P-type dopant material, respectively. The manufacturing process is then continued to complete the transistor 100 according to techniques well known to those skilled in the art.

As stated above, the pre-amorphization implanting process as depicted in Figure 1a is performed for the purpose of controlling the ion-channeling during the subsequent implanting steps to obtain doping profiles for both the halo structures and the source and drain regions that are as shallow as required in view of the reduced planar dimensions of the modern transistors. That is, by pre-amorphizing the substrate, the dopants implanted into the substrate during subsequent implanting processes are confined to shallow regions of a reduced depth close to the surface of the substrate.

However, as stated above, the prior art pre-amorphization process as depicted with reference to Figure 1a has the disadvantage that the ion-channeling during subsequent implanting processes cannot be adequately controlled in the horizontal

direction. Accordingly, the dopants implanted into the substrate during subsequent implanting processes may not be confined into shallow regions of predefined horizontal dimensions and the dopant concentration cannot be adequately controlled in correspondence of the channel edges. This in particular leads to reduced effective channel dimensions, with corresponding short-channel effects, affecting the transistor.

Accordingly, in view of the problems explained above, it would be desirable to provide a technique that may solve or at least reduce one or more of these problems. In particular, it would be desirable to provide a technique that allows the prevention and/or reduction of ion channeling during halo implantation and source and drain implantation processes in both the vertical and the horizontal direction.

#### SUMMARY OF THE INVENTION

In general, the present invention is based on the consideration that ion-channeling may be prevented or reduced in both the vertical and horizontal direction by performing a pre-amorphizing implantation step during which the substrate is exposed to an ion beam which is kept at a large tilt angle with respect to a direction perpendicular to the surface of the substrate.

For example, by performing a pre-amorphizing implantation step during which the ion beam is kept at a tilt angle of approximately  $40^\circ$  amorphous regions may be obtained extending partially beneath the gate insulation layer and the overlying polysilicon structure. This enables a good confinement of the following implantation steps in both the vertical and the horizontal direction. Accordingly, the dopants implanted into the substrate during subsequent implanting processes are confined to regions of both a reduced depth close to the surface of the substrate and predefined planar dimensions, with these shallow regions exhibiting a well defined dopant concentration in both the vertical and horizontal direction.

Moreover, the present invention is based on the further consideration that ion-channeling may be prevented or reduced in both the vertical and horizontal direction by performing an amorphizing implantation step during which the tilt angle is varied. For example, by dividing the amorphization implanting step into several periods and/or segments amorphous regions of a predefined profile may be obtained, thus

preventing ion-channeling during subsequent implantation steps in both the vertical and horizontal dimension, even if during these subsequent implantation steps the ion beam is tilted with respect to the surface of the substrate. For example, by dividing the amorphization step into several periods and/or segments, predefined regions of the substrate may be amorphized, depending on the tilt angles during the implantation periods, thus suppressing and/or minimizing the ion-channeling which usually arises in these regions.

According to one embodiment, the present invention relates to a method of forming at least one field-effect transistor on a semiconductive substrate. The method comprises forming at least one gate structure above an active region of the at least one transistor and implanting ions of at least one dopant material through the portions of the surface of the substrate not covered by the at least one gate structure, by exposing the surface of the substrate to at least one ion beam of the at least one dopant material so as to substantially amorphize the exposed portions of the surface to a predefined depth. Moreover, the ion beam is kept to a tilt angle with respect to a direction perpendicular to the surface of the substrate.

According to another embodiment, the present invention relates to a method of forming at least one field-effect transistor on a semiconductive substrate. The method comprises forming at least one polysilicon gate structure above an active region of the at least one transistor. Moreover, the method comprises implanting ions of at least a first dopant material during a first implantation step through the portions of the surface of the substrate not covered by the gate structure by exposing the surface of the substrate to at least one ion beam of the at least one dopant material so as to substantially amorphize the exposed portions of the substrate to a predefined depth. The method further comprises implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of the substrate not covered by the gate structure so as to form halo structures into the amorphized portions of the substrate. Moreover, during the first implantation step, the ion beam is kept at a tilt angle with respect to a direction perpendicular to the surface of the substrate.

According to a further embodiment of the present invention, a method of forming at least one field-effect transistor on a semiconductive substrate is provided. The method comprises forming at least one gate structure above an active region of the

at least one transistor and implanting ions of at least one dopant material through the portions of the surface of the substrate not covered by the at least one gate structure by exposing the surface of the substrate to at least one ion beam of the at least one dopant material so as to substantially amorphize the exposed portions of the substrate to a predefined depth. Moreover, the tilt angle of the ion beam with a direction perpendicular to respect to the surface of the substrate is varied according to a predefined time schedule comprising a plurality of implanting periods and the tilt angle is kept within a predefined range during each implanting period.

According to another embodiment, the present invention relates to a method of forming at least one field-effect transistor on a semiconductive substrate. The method comprises forming at least one polysilicon gate structure above an active region of the at least one transistor. Furthermore, the method comprises implanting ions of at least a first dopant material during a first implantation step through the portions of the surface of the substrate not covered by the gate structure by exposing the surface of the substrate to at least one ion beam of the at least one dopant material so as to substantially amorphize the exposed portions of the substrate to a predefined depth. The method further comprises implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of the substrate not covered by the gate structure so as to form halo structures into the amorphized portions of the substrate. During the first implantation step the tilt angle of the ion beam with respect to a direction perpendicular to the surface of the substrate is varied according to a predefined time schedule comprising a plurality of implanting periods and the tilt angle is kept within a predefined range during each implanting period.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages, objects and features as well as embodiments of the present invention are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings in which identical or corresponding parts are identified by the same reference numerals.

310303

Figures 1a to 1d represent a typical process sequence of a prior art method of forming the source and drain regions of a field-effect transistor comprising the step of implanting ions to amorphize the substrate.

Figure 1c' represent an enlarged view of the portion e depicted in Figure 1c.

Figure 2a to 2d represent a process sequence or a method of forming the source and drain regions of a field effect transistor comprising an amorphizing implantation process according to an illustrative embodiment of the present invention.

Figure 2d' represents an enlarged view of the portion e depicted in Figure 2d;

Figures 3a to 3c represent an amorphizing implantation process according to a further illustrative embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather that the described illustrative embodiments merely exemplify various aspects of the present invention, the scope of which is defined by the appended claims.

The present invention is understood to be of particular advantage when used for forming the active regions of field-effect transistors. For this reason, examples will be given in the following in which corresponding embodiments of the present invention are applied to the formation of the active regions of a field-effect transistor. However, it has to be noted that the use of the present invention is not limited to the formation of the active regions of field-effect transistors, but rather the present invention can be used in any other situation in which the realization of shallow doping profiles in a substrate and/or a workpiece is required. The present invention can be carried out in all those situations in which it is required to control the ion channeling during ion implantation steps with the purpose of forming well-confined doping profiles exhibiting a reliable dopant concentration in both the vertical and the horizontal direction. The present invention can be carried out in all those situations in which

optimum design of doped regions in a substrate is required. The present invention is therefore applicable in these situations and the source and drain regions of a field effect transistor depicted in the following illustrative embodiments are to represent any such portion and/or region of a substrate.

With reference to Figures 2a to 2d, an illustrative embodiment of the amorphizing method of the present invention will now be described.

In Figure 2a, reference 1 relates to a substrate on which a field-effect transistor 100 has to be formed, such as, for example, a PMOS, an NMOS, as used as a part of a CMOS pair. Reference 2 relates to isolation structures defining an active region of the transistor 100. The isolation structures 2 are provided as shallow-trench-isolation (STI) structures. However, other isolation structures, for instance LOCOS structures (local oxidation of silicon) could have been formed instead of STI structures. The isolation structures 2 essentially comprise an isolating material such as silicon dioxide, silicon nitride, or the like. Reference 3 relates to a polysilicon gate electrode, in the following also referred to as polysilicon gate line, formed on a gate insulation layer 6, patterned on the active region of the substrate 1. Moreover, in Figure 2a references 8da and 8db relate to corresponding ion beams to which the substrate 1 is exposed for the purpose of implanting ions through the portions of the surface of the substrate 1 not covered by the polysilicon line 3 and the underlying gate insulation layer 6 so as to damage the crystalline structure of the substrate 1. Finally, in Figure 2a reference 5d relates to regions of the substrate 1 in which the crystalline structure of the substrate has been damaged by exposing the substrate to the ion beams 8da and 8db. The regions 5d may either be continuous amorphous regions or may contain isolated crystal damages and/or non-overlapping amorphous regions, as will become more apparent in the following disclosure.

In Figures 2b to 2d, the features already described with reference to Figure 2a are identified by the same reference numerals.

In Figure 2b, reference 8h relates to an ion beam to which the substrate 1 is exposed for the purpose of implanting dopants into the substrate 1 so as to form halo structures into the damaged and/or amorphous regions 5d. These halo structures are identified in Figure 2b by the reference numeral 5h and may include angled halo implants although this is not shown in Fig. 2b.

In Figure 2c, reference 8e identifies an ion beam to which the substrate 1 is exposed for the purpose of forming the source and drain extension regions of the transistor 100. These source and drain extension regions are identified in Figure 2c by the reference numerals 5'S and 5'D, respectively.

In Figure 2d, reference 7SD identifies a further ion beam to which the substrate 1 is exposed during a further implantation process for the purpose of forming the source and drain regions of the transistor 100, with these source and drain regions being identified by the reference numerals 5S and 5D, respectively. Usually, a heavy implantation step is carried out for determining the final concentration of the source and drain regions 5S and 5D. For NMOS and PMOS type devices, this heavy implantation step is performed using an N-type and a P-type dopant material, respectively.

The manufacturing process for the formation of the active region of the transistor 100 depicted in Figure 2d may include the following steps.

As apparent from Figure 2a, a polysilicon gate structure, including the polysilicon line 3 and the gate insulation layer 6, is formed first according to well known techniques. The formation of the active regions normally starts after the polysilicon gate structure has been formed.

During a first implanting step according to the present invention, ions are implanted into the silicon substrate 1 so as to form amorphous regions 5d. For this purpose, the substrate 1 is exposed to an ion beam which is kept at a tilt angle with respect to a direction perpendicular to the surface of the substrate. In particular, a tilt angle may be selected between 10° and 80°, depending on the circumstances. If the implantation is performed at a large tilt angle as depicted in Figure 2a, the amorphous regions induced will extend well beneath the polysilicon gate structure. In contrast, when the implanting process is performed at an angle of about 10° or less, the amorphous regions will not extend beneath the gate structure to any great extent. Since the ion beam is kept at a tilt angle with respect to the surface of the substrate, the implanting process usually comprises two semi-periods, wherein the substrate 1 is rotated 180° about an axis perpendicular to the surface of the substrate at the end of the first semi-period and upon entering the second semi-period. That is the substrate 1 is exposed to the same ion beam during the first and second semi-

periods, and the ion beams 8da and 8db of Figure 2a simply indicate that the substrate has been rotated 180°.

Alternatively, the orientation of the ion beam may be varied at the end of the first semi-period and upon entering the second semi-period. In this case, the substrate 1 is exposed to two ion beams during the first and second semi-periods, respectively, and the ion beams 8da and 8db of Figure 2a indicate that the ion beam has been rotated.

Typical implant elements are xenon or other heavy inert ions such as germanium, silicon, argon, or combinations thereof, etc. at an implant energy in the range of approximately 50 to 150 keV.

Moreover, the amorphizing implantation step can be carried out so as to induce crystal damages and/or non-overlapping amorphous portions or the amorphizing implanting step can be carried out until these isolated amorphous portions overlap so that substantially uniform amorphous regions are formed. Typical implanting doses are in the range of approximately  $1 \times 10^{11} / \text{cm}^2$  to  $1 \times 10^{14} / \text{cm}^2$ .

Since the ion beam is kept at a tilt angle with respect to the surface of the substrate the amorphous regions 5d extend at least partially beneath the polysilicon gate structure. This allows a well-controlled suppression of the penetration depth both in lateral and vertical directions for subsequent implant steps of doping elements to form halo, and source and drain regions. In other words, the subsequent implanting structures will exhibit an optimum profile tailoring and a predefined dopant concentration both in the vertical and in the horizontal direction.

Once the amorphous regions 5d have been formed as described above, the manufacturing process is continued to form halo regions into the substrate during a subsequent implantation step as depicted in Figure 2b. To this end, the substrate 1 is exposed to an ion beam 8h and dopants are implanted into the amorphous regions 5d through those portions of the surface of the substrate 1 not covered by the polysilicon gate structure. The ion beam 8h may be kept either perpendicular to the surface of the substrate (0° tilt) or at a tilt angle with respect to the perpendicular to the surface of the substrate.



A tilt angle may be preferred in those circumstances in which halo regions are needed extending slightly into the channel region of the field-effect transistor 100, i.e. beneath the polysilicon gate structure. In contrast, in those circumstances in which halo structures are needed extending considerably in the vertical direction and less in the horizontal direction, a perpendicular ion beam is preferred. When a tilt angle is preferred, the implanting step is divided in two semi-periods, with either the substrate or the ion beam being rotated upon entering the second semi-period as explained above.

The halo regions 5h allow to prevent or to at least to reduce the short-channel effects, in particular the punch-through effect, in the transistor 100. The dopant concentration in the regions 5h as well as the implant energy and the dopant are selected depending on the type of transistor to be formed on the substrate 1. For instance, boron ions in NMOS and phosphorous ions in PMOS are implanted to form a halo punch-through suppression region in each device. Usually, phosphorous is implanted at 90 keV with a dose of  $2 \times 10^{13} \text{ cm}^{-2}$  at  $25^\circ$  tilt, in two segments, with the substrate rotated 180 between the two segments. Similar procedures are used for implanting boron.

A thermal treatment such as an annealing step is performed after the halo ion implantation step for diffusing the dopants into the substrate.

As stated above, due to the fact that the amorphous regions 5d have portions extending beneath the polysilicon gate structure, ion-channeling during the halo implanting step can be well controlled both in the vertical and the horizontal direction. That is, only very small amounts of the halo dopants may penetrate and/or diffuse into the channel region of the transistor 100 in a non-controlled way, or the halo dopants may even substantially completely be prevented from entering the channel region, but the penetration of the halo dopants into the channel region will be controlled and kept within predefined limits. Accordingly, the halo regions 5h may exhibit a desired doping profile in a substantially optimum manner, thereby tailoring both in the vertical and the horizontal direction i.e., the extension of the halo regions 5h into the substrate can be controlled in the vertical and in the horizontal direction and shallow halo structures can be obtained exhibiting a reliable dopant concentration.

The manufacturing process is then carried out to complete the transistor 100 according to techniques well known to those skilled in the art.

In particular, during a next step as depicted in Figure 2c a further ion implantation process is carried out for forming the source/drain extension regions 5'S and 5'D. To this end, a dose of approximately  $3 \times 10^{13}$  to  $3 \times 10^{14} \text{ cm}^{-2}$  dopant ions is implanted at low energy (3-5keV) by exposing the substrate 1 to an ion beam 8e. Usually, N-type and P-type dopant materials are used for NMOS and PMOS devices, respectively.

The source and drain regions 5S and 5D of the transistor 100 are then completed during a subsequent step as depicted in Figure 2d. In particular, dielectric sidewall spacers 4 are formed first on the sidewalls of the polysilicon line 3 according to well known techniques and a further heavy implantation step is carried out for implanting dopants into those regions of the substrate not covered by the polysilicon line 3 and the sidewall spacers 4. To this end, the substrate 1 is exposed to an ion beam 7SD which is usually kept substantially perpendicular with respect to the surface of the substrate 1. At the end of the heavy implantation step, the source and drain regions 5S and 5D are formed to exhibit a predefined dopant concentration. For NMOS and PMOS type devices, this heavy implantation step is performed using an N-type and P-type dopant material, respectively.

Also in the case of the implanting steps depicted in Figures 2c and 2d for forming the source and drain extension regions and the source and drain regions, ion channeling is reduced because of the amorphous regions 5d previously formed according to the present invention. In particular, the situation after formation of the source and drain regions will be the one depicted in Figure 2d' where there is depicted in an enlarged view the portion e defined by the dashed line in Figure 2d. as apparent from Figure 2d', neither the source region 5S nor the halo region 5h extend horizontally beyond the amorphous region 5d. That is, penetration of the dopants in the horizontal direction is controlled as well as in the vertical direction. Shallow junctions are therefore formed and the dopant regions exhibit a predefined dopant concentration and an optimum doping profile tailoring.

Once the source and drain regions 5S and 5D have been formed, the manufacturing process is continued to complete the transistor 100 according to techniques well known to those skilled in the art.

With reference to Figures 3a to 3d, a further illustrative embodiment of the method of the present invention for amorphizing a crystalline substrate will now be described.

In Figures 3a to 3d, the features already described with reference Figures 2a to 2d are identified by the same reference numerals. Moreover, in Figures 3a to 3c, references 8d11 and 8d12, 8d21 and 8d22, 8d31 and 8d32 relate to corresponding ion beams to which the substrate is exposed for the purpose of amorphizing the substrate. The tilt angles  $\alpha$ ,  $\beta$  and  $\gamma$  of these ion beams differ from each other.

During the implanting process according to the present embodiment for amorphizing the substrate, the tilt angle between the ion beam and the surface of the substrate 1 is not kept constant but is varied during the implanting process according to a predefined time schedule. That is, the implanting process comprises several implanting periods and/or segments, and the tilt angle between the ion beam and the surface of the substrate is varied from each segment to the subsequent segment. In particular, by choosing a non-constant timing for the different periods (at different implant angles of the implant process), predefined portions of the substrate may be amorphized to suppress or minimize ion-channeling arising in these regions during subsequent implanting processes.

Usually, the tilt angle may be varied between  $10^\circ$  and  $80^\circ$ . By selecting a predefined time schedule it becomes possible to realize amorphous zones having a particular shape. For instance, if the implanting with a tilt angle of about  $80^\circ$  is prolonged the amorphous regions will extend considerably beneath the polysilicon gate structure. On the contrary, if the implanting segment with a small tilt angle is prolonged, the amorphous regions will extend more in a vertical direction and less beneath the polysilicon gate structure.

In the illustrative embodiment depicted in Figures 3a to 3c, the method of implanting ions according to the present invention for amorphizing the substrate comprises three periods or segments. During a first period as depicted in Figure 3a, the ion beam is kept at a predefined tilted angle  $\alpha$  with respect to a direction perpendicular to the surface of the substrate 1. In the particular example depicted in Figure 1, the angle  $\alpha$  is about  $60^\circ$ . The tilt angle  $\alpha$  may either be kept substantially constant during the first implanting segment or it may be kept within a predefined range. The first implanting period may comprise two semi-periods, wherein the substrate is rotated  $180^\circ$  about

an axis perpendicular to the surface of the substrate at the end of the first semi-period and upon entering the second semi-period. In this case, the substrate is exposed to the same ion beam during the first and second semi-period, and the ion beams 8d11 and 8d12 in Figure 3a simply indicate that the substrate has been rotated  $180^\circ$ . Alternatively, the orientation of the ion beam can be modified, for instance by rotating the ion beam source, so as to expose the substrate to two ion beams 8d11 and 8d12 during the first and second semi-periods.

The implanting process is then continued by varying the tilt angle and implanting dopants during a second implanting segment as depicted in Figure 3b. In the particular example of Figure 3b, the tilt angle  $\beta$  is selected to about  $45^\circ$ . Again during the second period the tilt angle  $\theta$  can either be kept constant or kept within a predefined range. Moreover, the length of the second period may be either different from the length of the first period or may correspond to the length of the first period. Moreover, the second implanting period may be divided into two semi-periods and either the substrate may be rotated  $180^\circ$  or the ion beam source may be rotated. The ion beams 8d21 and 8d22 of Figure 3b indicate that the implanting period is divided into two semi-periods.

The implanting process is then continued with a third tilt angle  $\gamma$ ; in the particular example of Figure 3c a tilt angle  $\gamma$  of about  $30^\circ$  has been selected for the ion beams 8d31 and 8d32. Again, the third implanting period may be divided into two semi-periods with either the substrate 1 being rotated approximately  $180^\circ$  upon entering the second semi-period or the orientation of the ion beam being modified. The total length of the third period may correspond to the length of one or both of the first and second period. Alternatively, the total length of the third period may differ from the length of the first and second period.

At the end of the implanting process as depicted with reference to Figures 3a and 3d the situation on the substrate will be the one depicted in Figure 3d. In particular, as apparent from Figure 3d, the amorphous regions 5h exhibit a predefined shape depending on the time schedule selected for the amorphizing implantation process. accordingly, the amorphizing implanting process as depicted above allow to amorphize those portions of the substrate in which the need arises of preventing ion channeling.

31.03.03

It has to be noted that any number of implanting periods can be selected. For instance, two to ten periods of more can be provided, depending on the final shape required for the amorphous regions to be formed in the substrate 1.

The advantages of using an amorphizing implantation process according to the present invention are based on the fact that ion-channeling can be reduced and/or controlled during subsequent implanting processes both in the vertical and in the horizontal direction. This is accomplished by keeping the ion beam at a tilted angle between 10 and 80° during the amorphizing implantation process. The tilt angle may either be kept constant during the implanting process or may be varied according to a predefined time schedule.

It should be noted that a wide range of changes and modifications can be made to the embodiments described above. It is therefore also understood that are the claims, including all equivalencies, that define the scope of the invention.

## CLAIMS

1. A method of forming at least one field-effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of the at least one transistor;

implanting ions of at least one material through the portions of the surface of the substrate not covered by the at least one gate structure by exposing the surface of the substrate to at least one ion beam of the at least one material so as to substantially amorphize the exposed portions of the surface to a predefined depth;

wherein the ion beam is kept at a tilt angle with respect to a direction perpendicular to the surface of the substrate.

2. A method as claimed in claim 1, wherein the tilt angle is selected between 10° and 80°.
3. A method as claimed in claim 1 wherein the at least one material comprises heavy inert ions.
4. A method as claimed in claim 3, wherein the heavy inert ions comprise one of Xe, Ge, Si, Ar, or a combination thereof.
5. A method as claimed in claim 1, wherein the implanting energy is in the range of approximately 50 to 150 keV.
6. A method as claimed in claim 1, wherein the implanting dose is in the range of approximately  $1 \times 10^{11}/\text{cm}^2$  to  $1 \times 10^{14}/\text{cm}^2$ .
7. A method as claimed in claim 1, wherein the semiconductive material comprises one of Si and Ge.
8. A method as claimed in claim 1, wherein the field-effect transistor is one of an NMOS and a PMOS transistor.

9. A method as claimed in claim 1, wherein the substrate is rotated approximately 180° about an axis perpendicular to the surface at least once during implanting.

10. A method of forming at least one field-effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of the at least one transistor;

implanting ions of at least a first material during a first implantation step through the portions of the surface of the substrate not covered by the gate structure by exposing the surface of the substrate to at least one ion beam of the at least first material so as to substantially amorphize the exposed portions of the substrate to a predefined depth;

implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of the substrate not covered by the gate structure so as to form halo structures into the amorphized portions of the substrate;

wherein during the first implantation step the ion beam is kept at a tilt angle with respect to a direction perpendicular to the surface of the substrate.

11. A method as claimed in claim 10, wherein the tilt angle is in the range of approximately 10° to 80°.

12. A method as claimed in claim 10, wherein the at least first material comprises heavy inert ions.

13. A method as claimed in claim 12, wherein the heavy inert ions comprise one of Xe, Ge, Si, Ar or a combination thereof.

14. A method as claimed in claim 10, wherein the implanting energy during the first implantation step is kept in the range of approximately 50 to 150 KeV.

15. A method as claimed in claim 10, wherein the implanting dose during the first implantation step is in the range of approximately  $1 \times 10^{11}/\text{cm}^2$  to  $1 \times 10^{14}/\text{cm}^2$ .

16. A method as claimed in claim 10, wherein the semiconductive material comprises one of Si and Ge.
17. A method as claimed in claim 10, further comprising implanting ions of a second predefined conductivity type opposed to the first conductivity type during a third implantation step into the amorphized portions of the substrate.
18. A method as claimed in claim 17, further comprising forming spacer elements adjacent to a portion of the sidewalls of the gate structure; and  
  
implanting ions of a predefined conductivity type corresponding to one of the first and second conductivity types during a fourth implantation step through at least the portions of the surface not covered by the gate structures and the spacer elements.
19. A method as claimed in claim 10, wherein the field-effect transistor is one of an NMOS and a PMOS transistor.
20. A method as claimed in claim 10, wherein the substrate is rotated approximately 180° about an axis substantially perpendicular to the surface at least once during the first implantation step.
21. A method of forming at least one field-effect transistor on a semiconductive substrate, the method comprising:  
  
forming at least one gate structure above an active region of the at least one transistor;  
  
implanting ions of at least one material through the portions of the surface of the substrate not covered by the at least one gate structure by exposing the surface of the substrate to at least one ion beam of the at least one material so as to substantially amorphize the exposed portions of the substrate to a predefined depth;  
  
wherein the tilt angle of the ion beam with respect to a direction perpendicular to the surface of the substrate is varied according to a predefined time schedule comprising a plurality of implanting periods, and



wherein the tilt angle is kept within a predefined range during each implanting period.

22. A method as claimed in claim 21, wherein the tilt angle may be varied in the range of approximately  $10^{\circ}$  to  $80^{\circ}$ .
23. A method as claimed in claim 21, wherein the at least one material comprises heavy inert ions.
24. A method as claimed in claim 23, wherein the heavy inert ions comprise one of Xe, Ge, Si, Ar or a combination thereof.
25. A method as claimed in claim 21, wherein the implanting periods have different lengths.
26. A method as claimed in claim 21, wherein the tilt angle is substantially kept constant during each implanting period.
27. A method as claimed in claim 21, wherein the implanting energy is varied according to the predefined time schedule and wherein during each implanting period the implanting energy is kept within a predefined range.
28. A method as claimed in claim 27, wherein the implanting energy is varied in the range of approximately 50 to 150 keV.
29. A method as claimed in claim 21, wherein the implanting dose is varied according to the predefined time schedule and wherein the implanting dose is kept within a predefined range during each implanting period.
30. A method as claimed in claim 29, wherein the implanting dose is varied in the range of approximately  $1 \times 10^{11} / \text{cm}^2$  to  $1 \times 10^{14} / \text{cm}^2$ .
31. A method as claimed in claim 21, wherein the semiconductive material comprises one of Si and Ge.
32. A method as claimed in claim 21, wherein the field-effect transistor is one of an NMOS and a PMOS transistor.

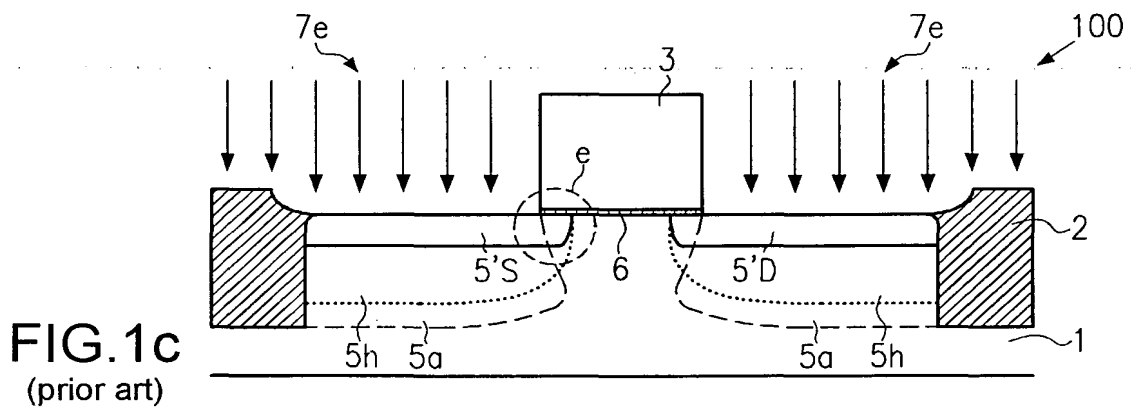
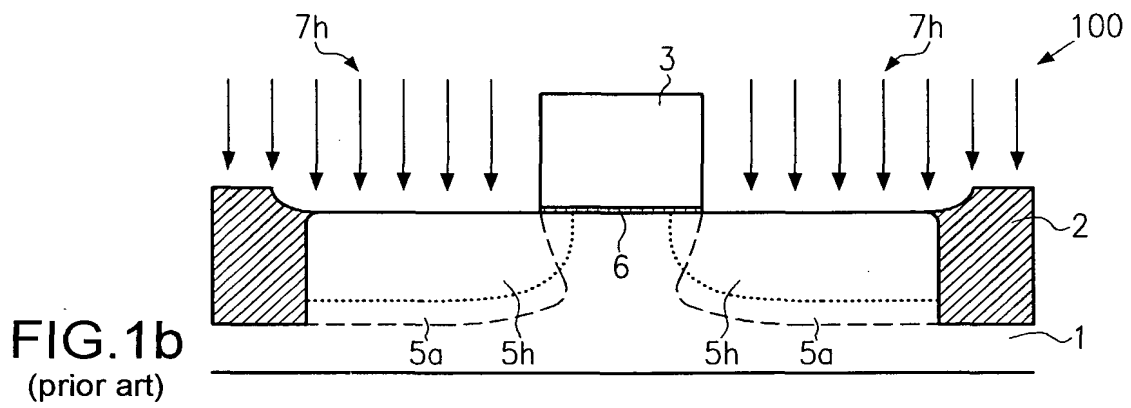
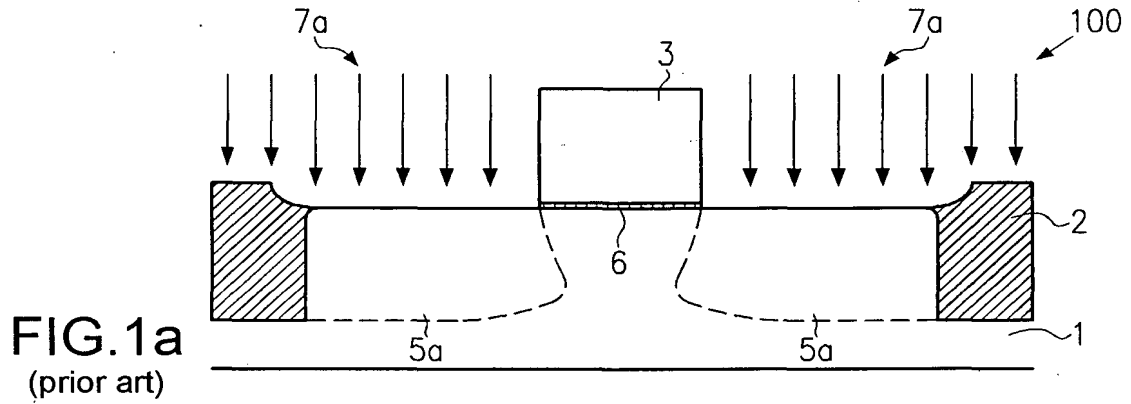
33. A method as claimed in claim 21, wherein the substrate is rotated approximately 180° about an axis substantially perpendicular to the surface at least once during each implanting period.
34. A method of forming at least one field-effect transistor on a semiconductive substrate, the method comprising:
- forming at least one gate structure above an active region of the at least one transistor;
  - implanting ions of at least a first material during a first implantation step through the portions of the surface of the substrate not covered by the gate structure by exposing the surface of the substrate to at least one ion beam of the at least one material so as to substantially amorphize the exposed portions of the substrate to a predefined depth;
  - implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of the substrate not covered by the gate structure so as to form halo structures into the amorphized portions of the substrate;
  - wherein during the first implantation step the tilt angle of the ion beam with respect to a direction perpendicular to the surface of the substrate is varied according to a predefined time schedule comprising a plurality of implanting periods, and
  - wherein the tilt angle is kept within a predefined range during each implanting period.
35. A method as claimed in claim 34, wherein during the first implantation step the tilt angle may be varied in the range of approximately 10° to 80°.
36. A method as claimed in claim 34, wherein the at least one material comprises heavy inert ions.
37. A method as claimed in claim 36, wherein the heavy inert ions comprise one of Xe, Ge, Si, Ar or a combination thereof.

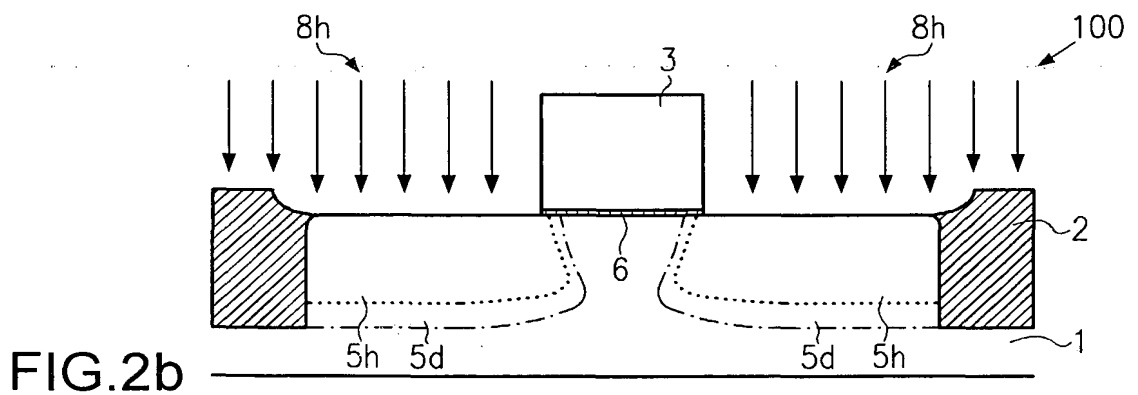
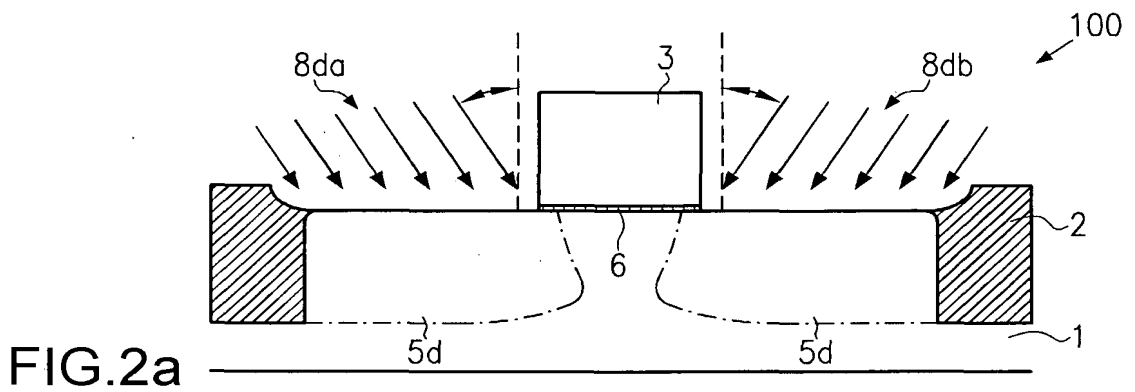
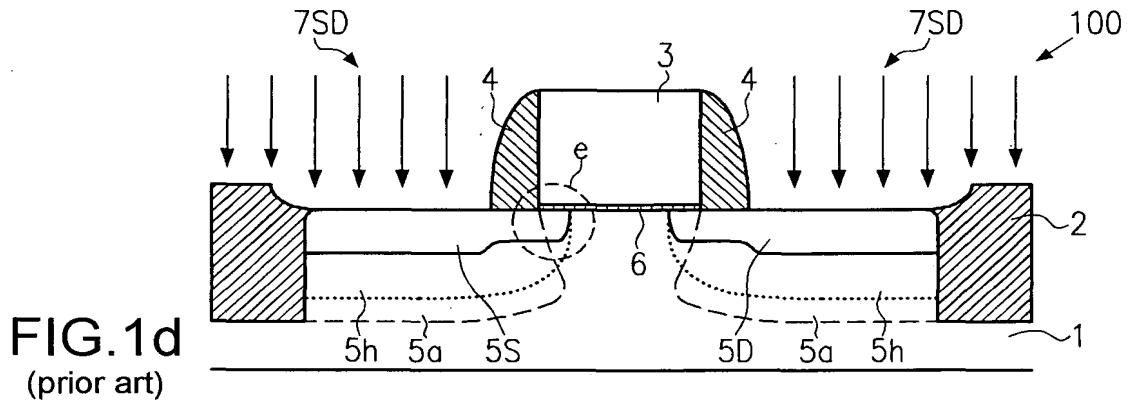
38. A method as claimed in claim 34, wherein the implanting periods have different lengths.
39. A method as claimed in claim 34, wherein the tilt angle is substantially kept constant during each implanting period.
40. A method as claimed in claim 34, wherein during the first implantation step the implanting energy is varied according to the predefined time schedule and wherein during each implanting period the implanting energy is kept within a predefined range.
41. A method as claimed in claim 40, wherein the implanting energy may be varied in the range of approximately 50 to 150 keV.
42. A method as claimed in claim 34, wherein during the first implantation step the implanting dose is varied according to the predefined time schedule and wherein the implanting dose is kept within a predefined range during each implanting period.
43. A method as claimed in claim 42, wherein the implanting dose may be varied in the range of approximately  $1 \times 10^{11}/\text{cm}^2$  to  $1 \times 10^{14} / \text{cm}^2$ .
44. A method as claimed in claim 34, wherein the semiconductive material comprises one of Si and Ge.
45. A method as claimed in claim 34, further comprising implanting ions of a second predefined conductivity type opposed to the first conductivity type during a third implantation step into the amorphized portions of the substrate.
46. A method as claimed in claim 45, further comprising forming spacer elements adjacent to a portion of the sidewalls of the gate structure; and  
  
implanting ions of a predefined conductivity type corresponding to one of the first and second conductivity types during a fourth implantation step through at least the portions of the surface not covered by the gate structures and the spacer elements.
47. A method as claimed in claim 34, wherein the field-effect transistor is one of an NMOS and a PMOS transistor.

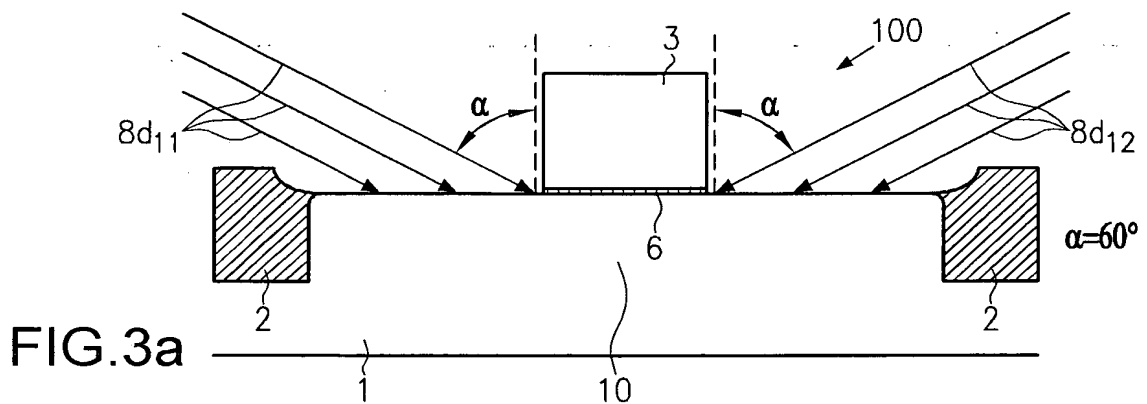
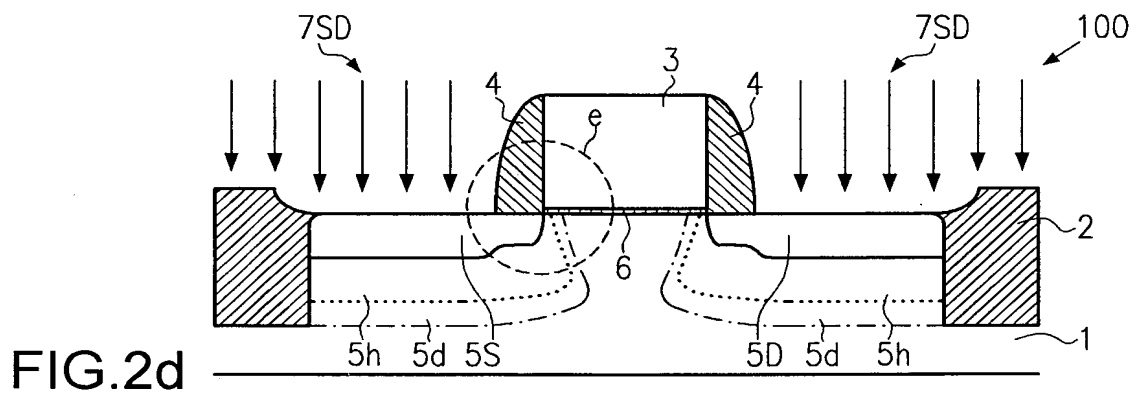
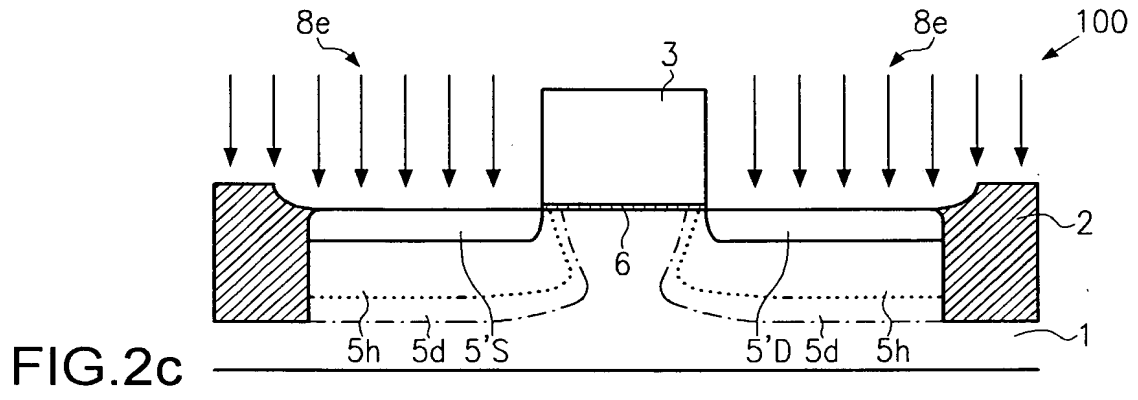
48. A method as claimed in claim 34, wherein during the first implantation step wherein the substrate is rotated approximately 180° about an axis substantially perpendicular to the surface at least once during each implanting period.

# **ABSTRACT**

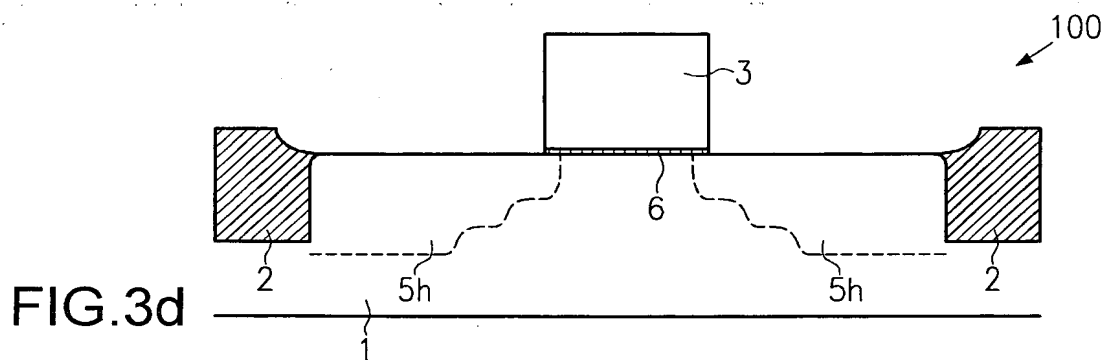
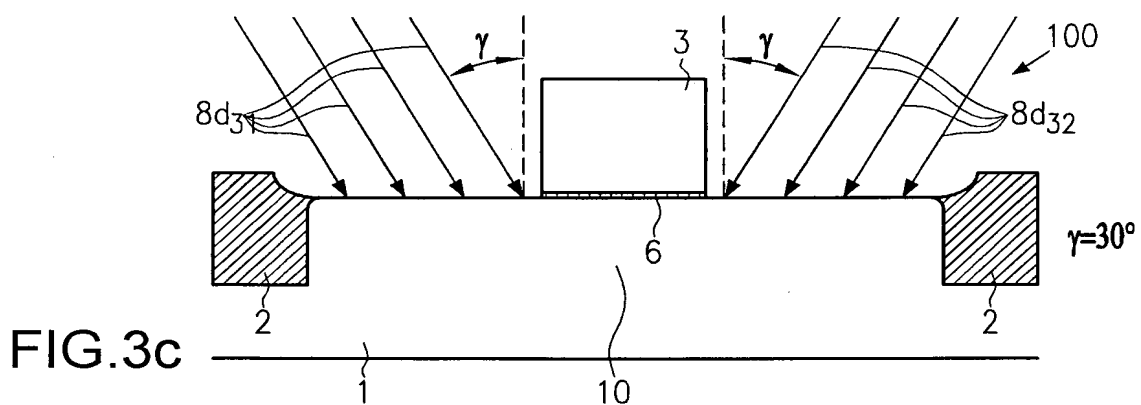
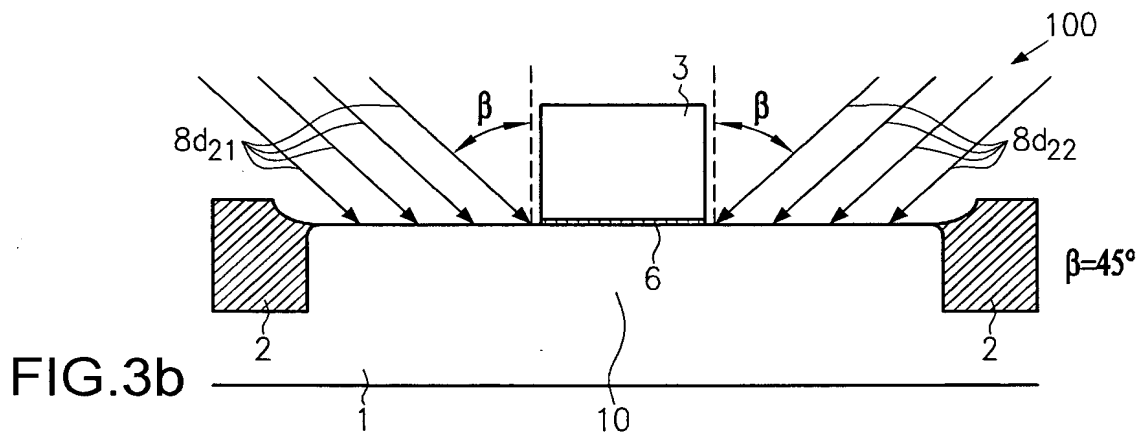
An implanting process for amorphizing a crystalline substrate is proposed according to the present invention. In particular, according to the present invention amorphous regions are formed in a substrate by exposing the substrate to an ion beam which is kept at a tilt angle between  $10^{\circ}$  and  $80^{\circ}$  with respect to the surface of the substrate. Accordingly, ion channeling during subsequent implanting processes is prevented not only in the vertical direction but also in the horizontal direction so that doped regions exhibiting optimum doping profile tailoring may be realized.











5/5

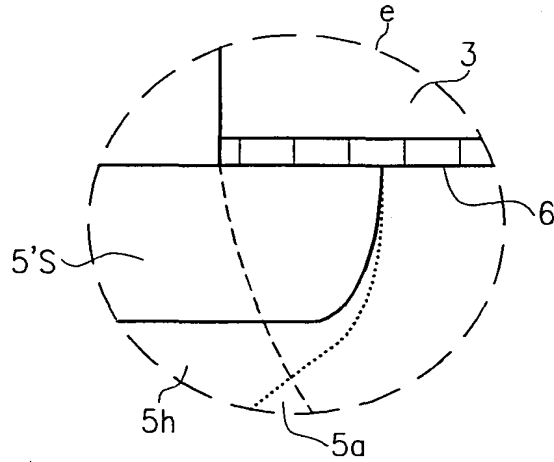


FIG. 1c'

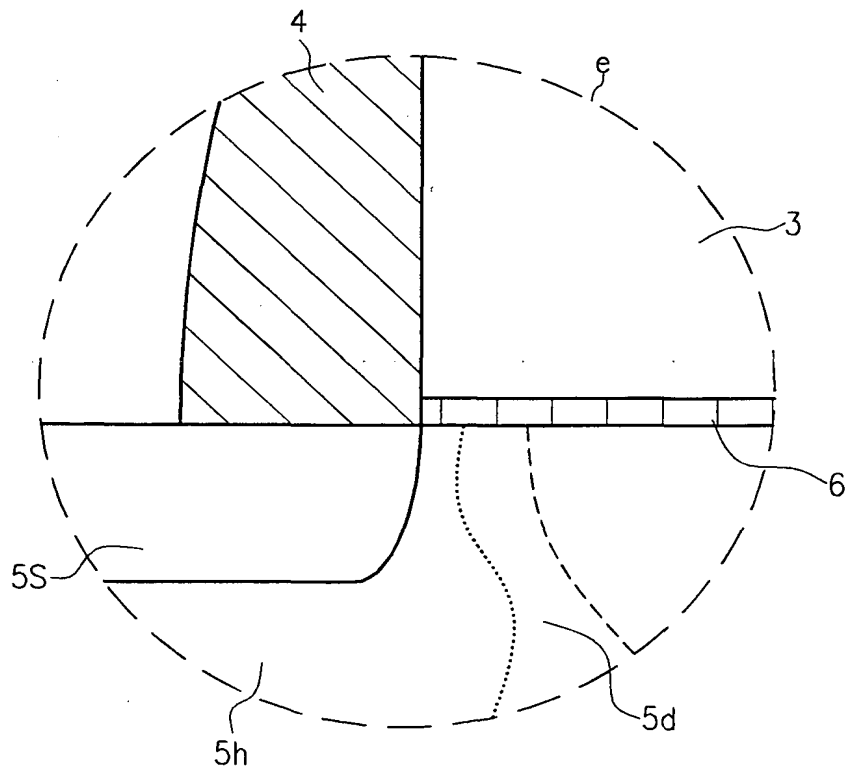


FIG. 2d'